A Single Chip 2-20 GHz T/R Module

M.J. Schindler, S.L. Chu, T.E. Kazior, A.M. Bertrand, K.M. Simon

Raytheon Company
Research Division
131 Spring Street Lexington, MA 02173

ABSTRACT

A single chip 2-20 GHz Transmit/Receive (T/R) module has been demonstrated. This MMIC includes a 4-stage power amplifier chain, a 4-stage low noise amplifier chain, and two T/R switches. A selective ion implantation process was used. One implant profile was optimized for low-noise operation, a second was optimized for power performance. All circuits were designed to be relatively insensitive to process variations to ensures adequate yield, despite the complexity of the chip. Distributed amplifiers are used throughout, and the T/R switches use a standard series-shunt FET configuration. All circuits have been miniaturized to keep the total chip size small. The entire T/R circuit measures only .143" x .193" (3.6 mm x 4.9 mm).

I. INTRODUCTION

Broadband MMIC component circuitry for use in T/R modules has been demonstrated, and has been extensively reported. [1-4] The assembly and testing of a large number of such MMICs into a module is difficult and costly. It is generally not possible, however, to combine all of these circuits within a single chip because different FET doping profiles are used for power and low noise devices. Further, the size of such a chip would be excessive for routine fabrication and assembly, and yield would be prohibitively low.

A selective ion-implantation process, named CODAMIT, has been developed.[5] This allows individual optimization of low noise and power devices. With such a technology, it becomes possible to manufacture a single chip T/R module with minimal compromises in performance.

II. FABRICATION

Our CODAMIT selective implant process was used to fabricate the single chip T/R module. In this process, refractory metal (Ti/W) is deposited and patterned to form a mask for an n^+ contact implant, and to define a marker to be used for aligning all subsequent layers. The metal is removed following the n^+ implant, except at the alignment marker locations. The n^+ implant has a peak doping of approximately $2x10^{18}$ cm^{-3}. The active layers for the low noise and power devices are seperately implanted through photo-resist. The power implant has a peak doping of approximately $2x10^{17}$ cm^{-3}. The low noise implant has a peak doping of approximately $3x10^{17}$ cm^{-3}. The implant profiles were designed so that a single shallow gate etch could be used to recess low pinch-off voltage low noise FETs and high pinch-off voltage power FETs simultaneously. Implant damage is used for mesa isolations.

Once all the implants are complete, a standard ohmic metalization and alloy are used. Then all gates are simultaneously defined with a single e-beam write. Gate length is 0.5 μm. Control of the implants and anneals has been adequate to ensure that both FET types come within 5% of their target currents.

Subsequent to the gate step, our standard MMIC process is used. A 2000 Å layer of Si_3N_4 is used both for FET passivation and the capacitor dielectric. A 4000 Å layer of tantalum metalization is used for small value resistors. A layer of 3 μm of Au is evaporated as a final metalization for transmission lines and spiral inductors. An image reversal lift-off process is used, and 5 μm widths and separations are achieved with high yield. For example, the spiral inductors in the single chip T/R circuit use 5 μm separations between turns. The wafer is thinned to 100 μm, and 20 μm x 100 μm via holes are plasma etched.

The performance of the low noise and power FETs made with this process rival that of conventional ion implanted MESFETs. The low noise FET provides 1.9 dB noise figure with 8 dB associated gain at 10 GHz at a 20% I_{dss} bias. The power FET provides 650 mW/mm power density (for a 480 μm device) simultaneously with 9 dB power gain and 41% power-added efficiency at 10 GHz.

III. DESIGN APPROACH

The block diagram of the T/R circuit is shown in Figure 1. Integrated on this single chip are a four-stage Transmit amplifier chain, a four-stage Receive amplifier chain, and two T/R switches.

The Transmit amplifier chain consists of four distributed amplifiers. As can be seen in Figure 1, three amplifier designs are used. The last stage is designed for highest output power. The middle two stages are a compromise, offering moderate power and gain with reduced power consumption. The first stage is designed for best gain and with a positive gain slope to compensate for the roll off in the subsequent stages.

The distributed amplifier is the only circuit type which has demonstrated good performance over the 2-20 GHz band.[1] Another advantage, particularly for this application, is their

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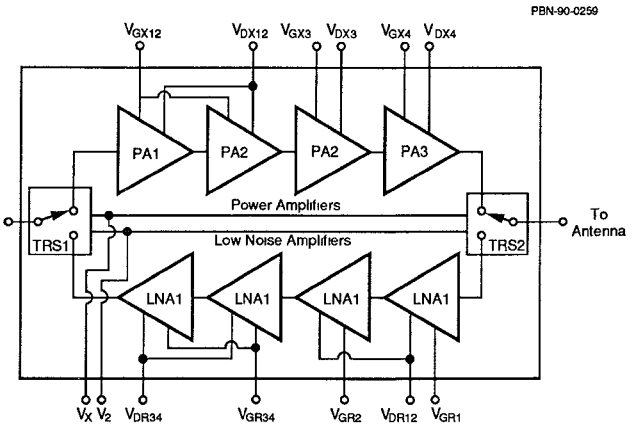

Figure 1. Block Diagram of the T/R Module.

relative insensitivity to process variations. A liability is their relatively large size.

Capacitive coupling of the FET gates in a distributed amplifier has been shown to allow the output power of the amplifier to be tailored.[1] This is because it allows a much greater range of adjustment in the periphery of the FETs. Capacitive gate coupling has been incorporated into all three power amplifier designs.

The power amplifiers are all designed to the schematic in Figure 2. The corresponding FET peripheries for each amplifier version are also indicated. PA3, the output amplifier, is designed for maximum power. It has a total of 1.5 mm of FET periphery. The preceding amplifiers, PA2 and PA1, provide lower output power and use smaller total FET periphery - 1.0 mm each. The input amplifier uses the same devices as the second and third stages, but is designed to provide extra gain at the high end of the band.

Particular care was taken to minimize the physical size of each amplifier. This was done by using minimum feature sizes and separations, and by using spiral inductors in place of moderate to long transmission line sections. The drain bias circuitry was also designed for minimum area. This circuit is evident in Figure 2, it essentially consists of a parallel connection of a large inductor (2 nH) and a drain terminating resistor, RF grounded through a large capacitor (15 pF). Such a bias circuit can be much smaller than more conventional ladder networks. The disadvantage of the bias circuit is in circuit performance. At the lower end of the frequency band, the impedance presented by the bias circuit is dominated by the inductor reactance. It was necessary to compensate for this in the design of the amplifiers, otherwise output power would have suffered, and a significant gain slope would have resulted.

It would have been possible to place most or all of the bias circuitry off of the MMIC, but this would have been counter to the spirit of a highly integrated MMIC. To do so would have required considerably more assembly time, and custom tuning of each assembly. The design philosophy was to keep all of the required bias and RF circuitry on the chip.

The Receive amplifier chain also consists of four distributed amplifiers. The distributed amplifier approach was selected for the same reason as in the Transmit amplifier: for inherent large bandwidth, and relatively low process sensitivity.

A single distributed amplifier design, shown in Figure 3, is used for all four Receive stages. In order to optimize the performance of the Receive chain, the first two stages are biased for low noise, and the second two stages are biased for high gain.

The total FET periphery of each stage is 0.64 mm. Only four FETs are used per stage. This was done soley to minimize size, even though noise performance was compromised, particularly at the high end of the band. The low noise amplifier was designed for flat gain, and equal noise performance at the band edges. Noise performance at the upper band edge is primarily controlled by the impedance presented to the FETs. Noise performance at the lower band edge is dominated by the noise

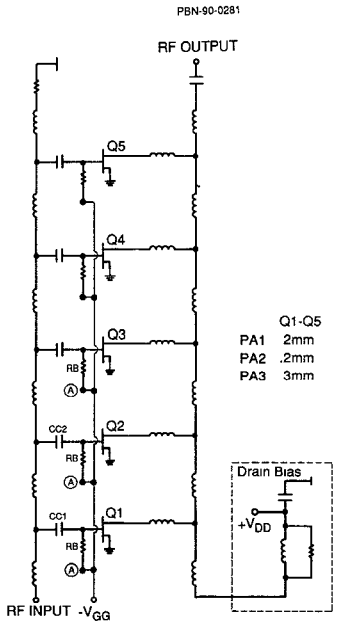

Figure 2. Schematic of the Power Amplifier Stages.

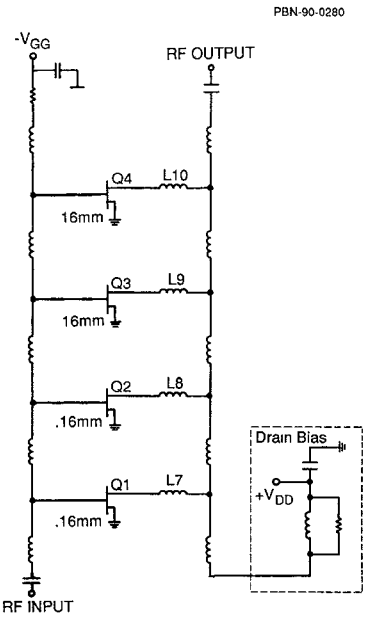

Figure 3. Schematic of the Low Noise Amplifier Stage.

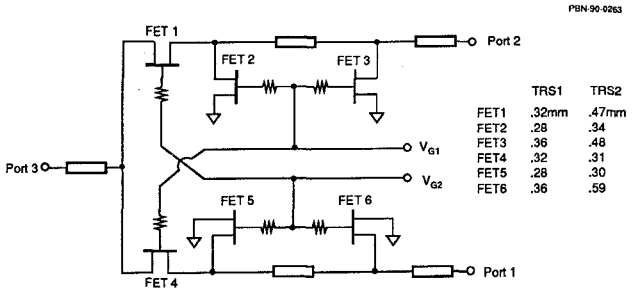

Figure 4. Schematic of the T/R Switches.

from the gate line terminating resistor. The value of this resistor may readily be increased to reduce noise, but at the cost of gain ripple.

The T/R switches are designed using a series/shunt switch FET circuit.[3] Like a distributed amplifier, such a circuit provides very large frequency bandwidth coverage, and is relatively insensitive to process variations. The back end switch (TRS1) is quite conventional in its design. To increase power handling, the front end switch (TRS2), uses larger FET peripheries in the Transmit arm than in the Receive arm. The two switch versions share a schematic, shown in Figure 4. FET peripheries are also indicated. It is evident that the peripheries of a number of FETs were increased in TRS2 to improve power handling.

Table 1
Summary of the T/R Module

Chip Size	0.143" x 0.194" 3.6 mm x 4.9 mm
Total Gate Periphery	11.5 mm
Number of FETs	44
Total Capacitance	190 pF
Number of Capacitors	44
Number of Resistors	69
Number of Spiral Inductors	60
Number of Via Holes	60
Number of Bias Terminals	13

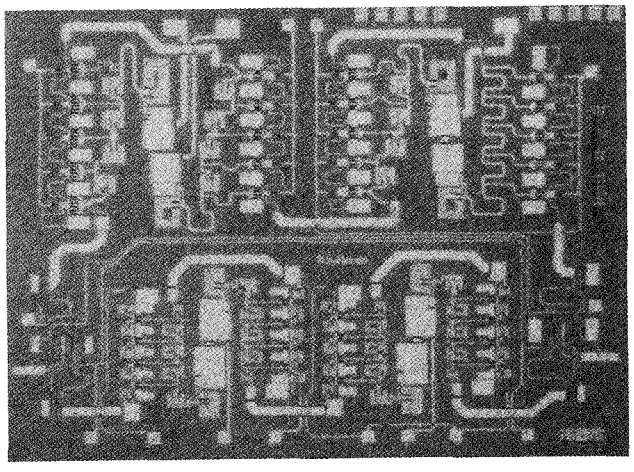

Figure 5. Photograph of the T/R Module.

The attributes of the single chip T/R circuit are summarized in Table 1. The actual chip is shown in Figure 5. It is evident the level of integration of the this MMIC is very high. The functions of the 13 bias terminals are indicated in Figure 1. It is possible to bias a number of these terminals in common. In actual use, generally only 9 bias inputs have been required.

IV. RESULTS

The results presented in this section are for the entire packaged T/R circuit. The loss of the switches and the packaging have not been removed from the data.

The maximum Receive gain of the T/R module is shown in Figure 6. The gain is better than 18 dB to 18 GHz, better than 16 dB to 20 GHz. The noise figure, shown in Figure 7, is 8.5-11 dB when biased at I_{dss}, 7.5-10 dB when biased at 50% I_{dss}. At 50% I_{dss}, gain drops 4-5 dB across the band. The individual LNA stages provide better than 6.8 dB noise figure with 5.5 dB of associated gain at 50% I_{dss} across the band, 6 dB noise figure and 4.5 dB gain at 25% I_{dss}. This is similar to the reported results for a broadband distributed LNA with MBE MESFETs.[4]

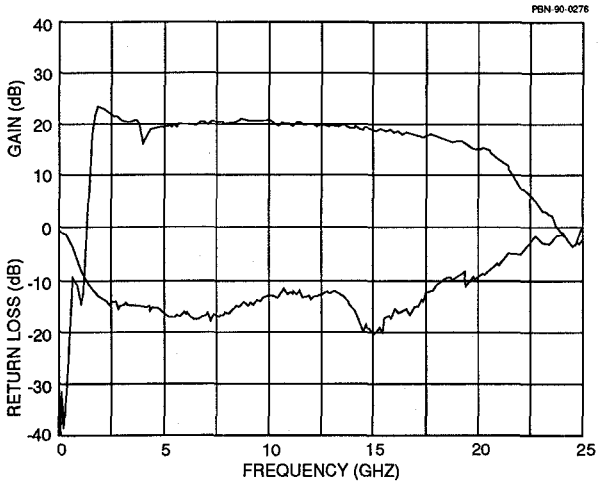

Figure 6. Receive Gain and Return Loss of the T/R Circuit.

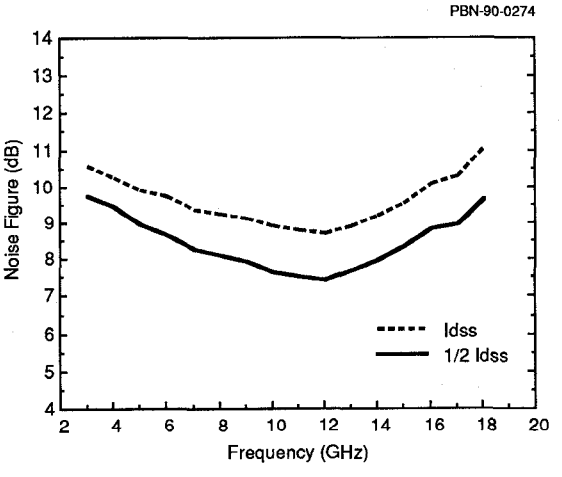

Figure 7. Receive Noise Figure of the T/R Circuit.

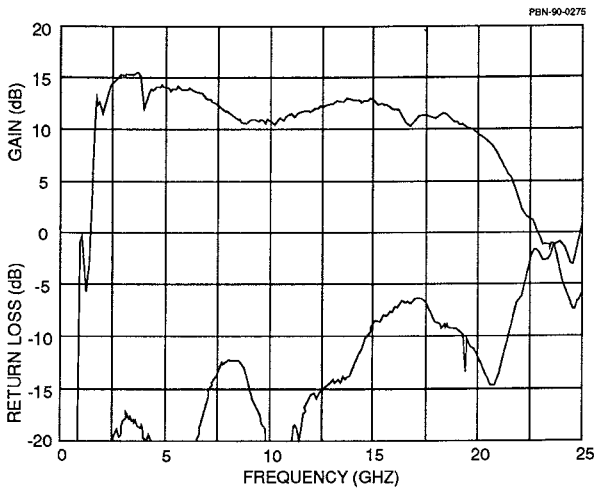

Figure 8. Transmit Gain and Return Loss of the T/R Circuit.

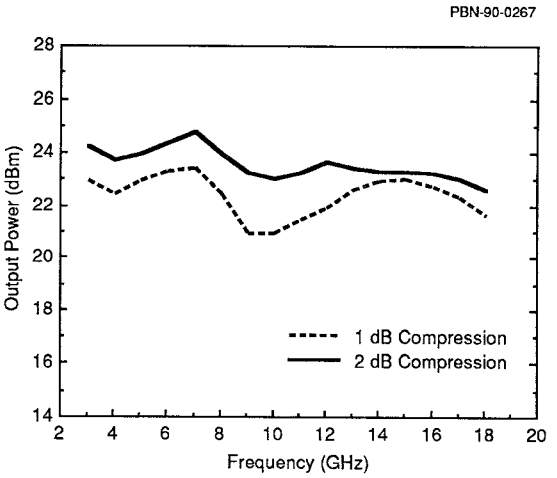

Figure 9. Transmit Power of the T/R Circuit.

The Transmit gain is shown in Figure 8. Over most of the 2-20 GHz band, in excess of 12 dB gain has been achieved. At 10 GHz gain is 11 dB, and at 20 GHz gain drops to 10 dB. Output power, shown in Figure 9, is 23-25 dBm (200-320 mW) at 2 dB gain compression, 21-24 dBm (125-250 mW) at 1 dB compression.

RF yield for the single chip T/R module has been as high as 18% on the best wafers, a remarkable acheivement given the complexity of the circuits.

V. SUMMARY

A highly integrated, single chip, 2-20 GHz T/R module has been demonstrated. A selective implantation process has been employed to provide devices optimized for noise and for power on the same chip. Circuits were designed to provide high RF yield, and to consume minimum chip area. A high level of circuit performance has been achieved.

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